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REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

[0004] State of the Art: Integrated semiconductor devices are typically constructed en masse on a wafer of silicon or gallium arsenide. Each device generally takes the form of an integrated circuit (IC) die, which is attached to a lead frame with gold wires. As shown in Figure 1, the die and lead frame are then encapsulated in a plastic or ceramic package, which is then recognizable as an IC "chip". IC chips come in a variety of forms, such as dynamic random access memory (DRAM) chips, static random access memory (SRAM) chips, read only memory[,] (ROM) chips, gate arrays, and so forth. The chips are interconnected in myriad combinations on printed circuit boards by a number of techniques, such as socketing and soldering.

[0006] Semiconductor devices typically take the form of a semiconductor die. The semiconductor die 11 is generally attached to a lead frame 13 within a package, by means of fine gold wires 15, as shown in Figure 1. [these] These fine gold wires function as lead frame connection wires. [the] The lead frame and die assembly is then encapsulated[,] in the form of the familiar integrated circuit "chip". The packaged chip is then able to be installed on a circuit board by any number of techniques, such as socketing and soldering.

[0011] The SIMM is a highly space-efficient memory board having no [on board] onboard address circuitry and which is designed to plug directly into the address, data and power-supply buses of a computer so that the [randomly-addressable] randomly addressable memory cells of the SIMM can be addressed directly by the computer's CPU rather than by a bank-switching technique commonly used in larger memory expansion boards. Memory cells on the SIMM are perceived by the computer's CPU as being no different than memory cells found on the computer's mother board. Since SIMMs are typically populated with byte multiples of DRAMs, for any eight bit byte or sixteen bit byte or word of information stored within a SIMM, each of the component bits will be found on a separate chip and will be individually addressable by column and row. One edge of a SIMM module is a card-edge connector which plugs into a

socket on the computer which is directly connected to the computer buses required for powering and addressing the memory on the SIMM.

[0015] In most cases, each of the module's decoupling capacitors are connected in parallel between the V_{CC} bus and the ground plane bus. As long as the dielectric of each of the eight capacitors is intact, the module is functional. However, a short in any one of the eight capacitors will result in the V_{CC} [buss] bus becoming shorted to the ground-plane bus, whereupon the module will begin to draw an inordinate amount of current which will invariably result in its destruction.

[0018] Most semiconductors, including all DRAMS, include capacitors. For example, a 4 megabit DRAM includes over 4 million capacitors [each]. For the purpose of storing individual bits of information, these capacitors are accessed by connections through access transistors and sense amplifiers[,] connected through a peripheral circuit. The present invention concerns adding filter capacitance to such devices in order to provide protection from voltage transients which may not be afforded by what may be millions of other capacitors on the semiconductor device.

[0019] Semiconductor circuit devices are designed with an architecture which places their functional circuitry within a confined area, usually rectangularly shaped. At the perimeter (either outside or inside) of the rectangularly shaped area [are] is a series of contact pads and a substantial amount of chip area which is occupied by conductor buses, but is unoccupied by active circuit devices. Unlike many of the circuit elements on a semiconductor circuit device, filter capacitors need not be built to precise specifications. It is, therefore, possible to utilize perimeter areas and portions of semiconductor chip areas which form major border areas between active portions of the semiconductor circuit device.

[0022] In accordance with the present invention, capacitance filtering is provided for a circuit having an array of similar semiconductor circuit devices, such as a SIMM [single in-line memory module] array of semiconductor circuit devices. The semiconductor circuit devices are formed with capacitors located primarily in border areas, including perimeter border areas and intermediate border areas.

[0033] Figure 12 shows a schematic block diagram representation of a semiconductor circuit device having an on-chip regulator.

[0039] The invention has been described in terms of connection to circuit buses which have external connections. It is possible that an additional circuit may be placed between the bus and an external connection. A likely example of such an additional circuit would be a [voltage regulating] voltage-regulating circuit. It is possible to connect the capacitor to a bus which extends between such an additional circuit and a main portion of the integrated circuit device.

[0040] The present embodiment contemplates the use of [N channel] N-channel capacitors, with V_{ss} connected to the active area of the substrate 30' [x] and V_{cc} connected to poly 75. This is shown in Figure 6. It is possible to construct [P channel] P-channel capacitors with V_{cc} connected to the active area of the substrate 30" and V_{ss} connected to poly 85. This is shown in Figure 7. Each of these is an enhancement mode capacitor, which has a preferential voltage polarity. It is also possible to form these capacitors as depletion mode capacitors.

[0042] Figure 9 shows a SIMM (single in-line memory module) board 101, which consists of a printed circuit board 103, on which [are] is mounted a plurality of semiconductor memory devices such as DRAMs 105. The printed circuit board 103 includes an edge connector 107, which extends from the printed circuit board 103 in order to permit the SIMM board 101 to be plugged into a computer bus (not shown) on a computer. The computer bus has a capability of addressing the DRAMs 105 on the board in predetermined sequence, as defined by the SIMM protocol. Typically, an entire row of DRAMs 105 is simultaneously addressed to obtain a byte of information. Other addressing schemes are, of course, possible.

[0043] Figures 10 and 11 show the use of capacitors on DRAMS 105. A SIP (single in-line package) board 111, as shown in Figure 11, and similar boards[,] which use a connector to connect an array of similar components with parallel address circuitry through a connector may also be used with the invention.[.]

IN THE CLAIMS

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Amended) A semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising:
a carrier substrate; and
a semiconductor device secured and operably coupled to the carrier substrate and including:
a semiconductor substrate having active circuit devices thereon; and
an on-chip capacitor including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active circuit devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

5. (Amended) The semiconductor device of claim 3, wherein the on-chip capacitor includes a first node and a second node, one node of the first and second nodes comprising a poly layer and the other node of the first and second nodes comprising a channel.

10. (Amended) The semiconductor device of claim 8, wherein the at least one capacitor includes a first node and a second node, one node of the first and second nodes comprising a poly layer and the other node of the first and second nodes comprising a channel.